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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/862,523	05/22/2001	Steven Derrick Clynes	TI-32423	1218

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EXAMINER
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MOE, AUNG SOE

ART UNIT	PAPER NUMBER
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2685

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/862,523

Applicant(s)

CLYNES ET AL.

Examiner

Aung S. Moe

Art Unit

2685

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,3-13,17,18 and 20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 3-13, 17, 18 and 20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments filed on 8/5/2005 have been fully considered but they are not persuasive.

In page 7 of the remarks, the Applicant alleged that the elements A, B and C refer to "luminance value" as shown in Figs. 3a-3j of Chen '578 is not pixel values.

In response, the Examiner respectfully disagrees because Chen '578 clearly stated in col. 6, lines 30+ that "For instant in Figure 3a through 3j, each drawing illustrates a group of three neighboring pixels in the image signal. The pixels are illustrated as bars, which bars correspond to the luminance value for the given pixel. For instant in Figure 3a, the pixel B 52 has a luminance value greater than that of the pixel A 50 and the pixel C 54." In view of this, it is cleared that as light reaches a pixel (i.e., noted the sensor array 6 and the pixel arrays as shown in Figs. 4a-4c and 6), that pixel converts the light into an electrical signal that is indicative of the light's intensity (i.e., "luminance value" as shown in Figs. 3a-3j) to shown the image changes from dark to light, and this is clearly anticipated the "pixel values" as required by the present claimed invention.

Furthermore, the Applicant alleged that Chen '578 does not show or suggest the presently claimed invention including the method step of detecting the lowest pixel value among the adjacent pixels.

In response, the Examiner respectfully disagrees because Chen '578 clearly shown, e.g., in Figs. 3a-3j, how to determining the lowest pixel value among the adjacent pixels. For example, it is clear form Figs. 3a-3j of Chen '578 that one of the lowest pixel value among the

Art Unit: 2685

adjacent pixels is considered to be the lowest pixel value, and this is further evidenced by Chen '578 as discussed in col. 6, lines 30+. In particular, Chen '578 stated in col. 6, lines 30+ that in FIG 3a, the pixel B 52 has a luminance value greater than that of the pixel A 50 and the pixel C 54 has a luminance value greater than that of the pixel B 52, and this clearly implied that the pixel value of "A 50" is determined to be the lowest among the adjacent pixels "B 52" and "C 54".

In addition, Chen '578 discloses the steps of resetting the process pixel value to a new process pixel value (i.e., Replacing the pixel value B with a new pixel value  $B_{corrected}$ ; see col. 9, lines 45+) when the process pixel value is a predetermined value (i.e., noted the value as shown in Fig. 3j) lower than the lowest pixel value (noted from Fig. 3j, a predetermined value is lower than the lowest pixel value A, then the pixel value B is replaced with a new pixel value  $B_{corrected}$ ; see col. 9, lines 45+).

In view of the above, the Examiner continues to assert that Chen '578 does in fact show the present claimed invention as required, and the Examiner will maintain the previous Final Office.

Applicant's arguments, see page 6 of the remarks, filed on 8/5/2005, with respect to 35 U.S.C. 112 have been fully considered and are persuasive. The 35 U.S.C. 112 rejection of claim 17 has been withdrawn.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3-11, 17-18 and 20 are rejected under 35 U.S.C. 102(a) as being anticipated by Chen et al. (EP 1,045,578 A2).

Regarding claim 1, Chen '578 discloses a method of pixel filtering for CMOS imagers (Figs. 1 & 2; col. 4, lines 35+), comprising: scanning each of a plurality of pixels within a block (i.e., noted the pixel block as shown in Fig. 4a-4c; col. 7, lines 10+); designating a pixel as a process pixel (i.e., noted the B pixels as shown in Figs. 3a-4c; see col. 7, lines 10+), the process pixel having adjacent pixels (i.e., noted the A and C pixels as shown in Figs. 3a-4c; see col. 7, lines 10), the process pixel having a process pixel value (i.e., noted the pixel value of the middle pixel B as shown in Figs. 3a-4c; see col. 7, lines 10+), each of the adjacent pixels having an adjacent pixel value (i.e., noted the pixel values of the adjacent pixels A and B as shown in Figs. 3a-4c; see col. 7, lines 1+); and comparing the process pixel value to at least one adjacent pixel value (i.e., col. 6, lines 30+, col. 7, lines 1+, col. 8, lines 5+); and detecting a lowest pixel value among the adjacent pixels (i.e., as shown in Figs. 3a-3j, the lowest pixel values of the adjacent

Art Unit: 2685

pixels A and C are respectively determined by the imaging logic 8; see col. 6, lines 30+, col. 7, lines 10+ and col. 8, lines 5+ and col. 9, lines 45+).

Regarding claim 3, Chen '578 discloses wherein comparing compares the process pixel value to a lowest pixel value (as shown in Figs. 3a-3j, the defective-pixel filter 34 of the imaging logic 8 compared the lowest pixel value of the adjacent pixels A/C with the middle pixels B; see col. 8, lines 1+ and col. 9, lines 15+).

Regarding claim 4, Chen '578 discloses further comprising resetting the process pixel to a new pixel value (i.e., as discussed in col. 9, lines 45+, that if the condition of the pixel values are determined to be as shown in Figs. 3g and 3j, then the process pixel B is reset, e.g., replaced, by a new pixel value B<sub>corrected</sub>; see col. 9, lines 45+).

Regarding claim 5, Chen '578 discloses wherein the new pixel value is the average pixel value of the adjacent pixel values (i.e., col. 9, lines 50+).

Regarding claim 6, Chen '578 discloses further comprising detecting a highest pixel value among the adjacent pixels (i.e., noted the pixel values of pixel 54 as shown in Figs. 3g and 3j).

Regarding claim 7, Chen '578 discloses wherein comparing compares the process pixel value to a highest pixel value (i.e., noted from Figs. 3a-3j and 5 that the defective-pixel filter 34 of the imaging logic 8 compared the highest pixel value of the adjacent pixels A/C with the middle pixels B; see col. 8, lines 1+ and col. 9, lines 15+).

Regarding claim 8, Chen '578 discloses further comprising resetting (i.e., Replacing the pixel value B with a new pixel value  $B_{\text{corrected}}$ ; see col. 9, lines 45+) the process pixel value (i.e., the B pixel value as shown in Fig. 3j) when the process pixel value is a predetermined value (i.e., noted the value as shown in Fig. 3j) lower than the lowest pixel value (noted from Fig. 3j, a predetermined value is lower than the lowest pixel value A, then the pixel value B is replaced with a new pixel value  $B_{\text{corrected}}$ ; see col. 9, lines 45+).

Regarding claim 9, Chen '578 discloses further comprising resetting the process pixel value (i.e., Replacing the pixel value B with a new pixel value  $B_{\text{corrected}}$ ; see col. 9, lines 45+) when the process pixel value is a predetermined value (i.e., noted the value as shown in Fig. 3g) greater than the highest pixel value (noted from Fig. 3g, a predetermined value is greater than the highest pixel value C, then the pixel value B is replaced with a new pixel value  $B_{\text{corrected}}$ ; see col. 9, lines 45+).

Regarding claim 10, Chen '578 discloses further comprising exposing an array to a light source so as to cast an image on the array (Fig. 1, the sensor array 6; col. 5, lines 20+), the array having at least one block (i.e., noted the block as shown in Fig. 4).

Regarding claim 11, Chen '578 discloses wherein the array is generally grid-shaped (i.e., noted that an array of CMOS sensor cells contain a matrix of pixel array generally formed as a grid-shape).

Regarding claim 17, Chen '578 discloses a method of on-chip pixel filtering for CMOS imagers (Figs. 1 & 2; col. 4, lines 35+), comprising:

scanning each of a plurality of pixels within a block for a pixel value (i.e., see Figs. 3a-4c; col. 7, lines 5+); loading a pixel value into a register (Fig. 5; col. 7, lines 35+ and col. 8, lines 5+); using filter logic (34) to designate a pixel as a process pixel (i.e., noted that the pixel B is designated by the filter logic 34 as a process pixel; see col. 6, lines 30+), the process pixel having adjacent pixels (i.e., noted the pixels A and C as shown in Fig. 3a-4c), the process pixel having a process pixel value (i.e., noted the process pixel values of pixel B as shown in Figs. 3a-3j), each of the adjacent pixels having an adjacent pixel value (i.e., noted the pixel values of the adjacent pixels A and C as shown in Figs. 3a-4c; see col. 7, lines 1+); and using filter logic (34) to compare the process pixel value to at least one adjacent pixel value;

wherein the filter logic (34) compares the process pixel value (i.e., the middle pixel value B as shown in Figs. 3g and 3j) to a lowest pixel value (i.e., noted the lowest pixel value is determined to have a shorter bar as shown in Figs. 3g and 3j), further comprising: detecting the lowest pixel value among the adjacent pixels (i.e., noted from Figs. 3a-3j, the lowest pixel values are determined by the filter logic 34 and the system controller 28); and resetting the process pixel value to a new process pixel value (i.e., Replacing the pixel value B with a new pixel value  $B_{corrected}$ ; see col. 9, lines 45+) when the process pixel value is a predetermined value (i.e., noted the value as shown in Fig. 3j) lower than the lowest pixel value (noted from Fig. 3j, a predetermined value is lower than the lowest pixel value A, then the pixel value B is replaced with a new pixel value  $B_{corrected}$ ; see col. 9, lines 45+).

Regarding claim 18, Chen '578 discloses wherein the filter logic compares the process pixel value to a highest pixel value, further comprising: detecting the highest pixel value among the adjacent pixels; and resetting the process pixel value to a new process pixel value when the



Art Unit: 2685

process pixel value is a predetermined value higher than the highest pixel value (i.e., Fig. 5; col. 6, lines 30+, col. 7, lines 1+, col. 8, lines 5+).

Regarding claim 20, Chen '578 discloses wherein the new process pixel value is the average pixel value of the adjacent pixel values (i.e., see col. 9, lines 45+).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen '578 in view of Watanabe et al. (U.S. 6,002,433).

Regarding claims 12 and 13, it is noted although Chen '578 shows the use of block of sensor (i.e., see Figs. 4a and 6), Chen '578 does not explicitly state that the block is generally grid-shaped and has nine pixels as required by the present claimed invention.

However, the above-mentioned claimed limitations are well known in the art as evidenced by Watanabe '433. In particular, Watanabe '433 teaches the use of block of nine pixels arranged in grid-shaped for detection of defective pixel with high precision (i.e., see Fig. 8; col. 1, lines 30-35 and col. 2, lines 55-60) in the imaging system.

Art Unit: 2685

In view of the above, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the system of Chen '578 as taught by Watanabe '433 so that detection of defective pixel can be carried out at high speed with high precision as suggested by Watanabe '433 (i.e., see col. 16, lines 5+).

### *Conclusion*

6. This is an RCE of applicant's earlier Application No. 09/862,523. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

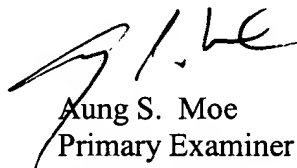
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Art Unit: 2685

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aung S. Moe whose telephone number is 571-272-7314. The examiner can normally be reached on Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward F. Urban can be reached on 571-272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Aung S. Moe  
Primary Examiner  
Art Unit 2685

A. Moe  
September 6, 2005